REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-5 and 7-15 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejection in view of the amendments and remarks as set forth below.

Changes to the Specification

Applicants have amended the specification on page 7 to correct an error in terminology. In the paragraph describing Fig. 7, the channels which are in a floating state are clearly defined as being every third channel, starting with the 2nd, then the 5th, 8th, and so on to the 383rd channel. However, in the final sentence, this has been summarized as the (3n-1)th channels. Since n has been defined in the claims as the number of floating channels, the term (3n-1)th would then only refer to the 383rd channel. This is clearly not the intent. In order to properly state the relationship, Applicants have added "2nd, 5th..." to correct this term. The same terminology has also been used in claims 1 and 5. Applicants wish to point out that this change does not constitute any new matter. In fact, it is to correct what is a clear error in the terminology, which had not previously been noted.

Allowable Subject Matter

It is gratefully acknowledged that the Examiner considers the subject matter of claims 12 and 13 as being allowable if rewritten in independent form. Claims 12 and 13 have been rewritten in independent form including the limitations of independent claims 1 and 5 from which they depend. However, intervening claims 2 and 9 have not been included, since they are believed to be unnecessary for patentability. Accordingly, claims 12 and 13 are now in condition for allowance.

Rejection under 35 U.S.C. § 103

Claims 1-11, 14 and 15 stand rejected under 35 U.S.C. § 103 as being obvious over the admitted prior art in view of Oh et al. (USP 5,856,818). This rejection is respectfully traversed.

The Examiner points out that the admitted prior art shows a liquid crystal panel having gate and data lines which define sub-pixel regions, with gate driving integrated circuits on either side and a plurality of data drive circuits on the upper portion of the panel where each of the data drive integrated circuits has m number of channels. The Examiner relies on Oh et al. to show that more than three data drive ICs in a bank can be used. However, Oh et al. does not relate to a quad-type LCD driver. Also, Fig. 11 of Oh et al. shows only a plurality of data drive ICs. The Examiner further admits that

neither the admitted prior art nor Oh et al. show the floating channels as defined. However, the Examiner feels it would have been obvious to spread out the floating channels over the entire drive.

Applicants disagree with the Examiner's belief that the claimed discussion of the floating channels would be obvious. It should be pointed out that the discussion of the channels makes it clear that every third channel is floating. This is not merely to spread out the channels, but is used as part of the approach to obtain the specific polarity in the pixels, as shown in Figs. 8A-8C. Thus, the integrated circuit arrangement normally provides alternating polarity signals along consecutive lines. By having the center channel in each group of three being floating, the 1st and 3rd channels have the same polarity and the 1st and 3rd channels in the next group have the same polarity, but opposite to the first group. Thus, the arrangements shown in Figs. 8A and 8B is accomplished in a simple fashion. Accordingly, the definition of the floating channels does not merely spread out the floating channels along the entirety of the m channels available, but occurs in a specific relationship in order to obtain the desired signal of pairs of the same polarity separated by pairs of opposite polarity. This concept is not seen in either the admitted prior art or in the Oh et al. reference, as admitted by the Examiner, and would not be obvious thereover. One skilled in the art would not see to remove the specific channels indicated even if he recognized the need to spread the floating channels

throughout the entire integrated circuit. Accordingly, Applicants submit that claim 1 is not obvious over the combination of the admitted prior art and the Oh et al. reference.

Claims 2-4, 8 and 14 depend from claim 1 and as such, are also considered to be allowable.

Claim 5 is an independent claim, which has now been amended to include the limitations previously found in claim 6. Claim 5 now also discusses the arrangement of the floating channels in the same fashion as claim 1, and therefore the remarks of claim 1 above also apply to claim 5. Accordingly, claim 5 is likewise considered to be allowable.

Claims 7, 9-11 and 15 depend from claim 5 and as such, are also considered to be allowable.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the references relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse (Reg. No. 27,295) at the telephone number of the undersigned below, to

conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fee required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By: Jett L. Ime #41,458
James T. Eller, Jr.
Reg. No. 39,538

JTE/RFG/gf
(703) 205-8000
3430-0164P

P.O. Box 747
Falls Church, Virginia 22040-07047